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	APPLICANT Jingo NAKANISHI	
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
M	5,703,511	12/30/1997	OKAMOTO	327	157	

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EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No
M	11-225069	08/17/1999	Japan (w/ English Abstract)				
M	07-177027	07/14/1995	Japan (w/ English Abstract)				
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

M	"MONOLITHIC PHASE-LOCKED LOOPS AND CLOCK RECOVERY CIRCUITS Theory and Design", Behzad Razavi, IEEE PRESS, 1996

EXAMINER	DATE CONSIDERED
[signature]	3/6/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.